

IN THE CLAIMS:

Please cancel claims 25-36 without prejudice, and
amend the following claims:

C1

1 1. (Amended) A semiconductor integrated circuit
2 comprising:
3 a first logic gate using, as an operation power source
4 in an active operation mode, a first pair of potentials
5 having a relatively small potential difference; and
6 a second logic gate using, as an operation power
7 source in said active operation mode, a second pair of
8 potentials having a relatively large potential difference,
9 wherein substrate potentials of MIS transistors are
10 commonly used by said first and second logic gates.

C2

1 6. (Amended) A semiconductor integrated circuit
2 comprising:
3 a first logic gate using, as an operation power source
4 in an active operation mode, a first pair of potentials
5 having a relatively small potential difference; and
6 a second logic gate using, as an operation power
7 source in said active operation mode, a second pair of
8 potentials having a relatively large potential difference,

9 wherein said first and second logic gat s have MIS
10 transistors, and a well region in which an MIS transistor
11 of said first logic gate is formed and a well region in
12 which an MIS transistor of said second logic gate is formed
13 are made common for each conduction type.

1 7. (Amended) A semiconductor integrated circuit
2 comprising:

C2
concl
3 a first logic gate using, as an operation power source
4 in an active operation mode, a first pair of potentials
5 having a relatively small potential difference; and

6 a second logic gate using, as an operation power
7 source in said active operation mode, a second pair of
8 potentials having a relatively large potential difference,

9 wherein said first and second logic gates have MIS
10 transistors, and a well region in which an MIS transistor
11 of said first logic gate is formed and a well region in
12 which an MIS transistor of said second logic gate is formed
13 are electrically connected for each conduction type.

1 12. (Amended) A semiconductor integrated circuit
2 comprising:

C3
3 a first logic gate using, as an operation power source

C2
Coul

4 in an active operation mode, a first pair of a high
5 potential and a low potential; and
6 a second logic gate using, as an operation power
7 source in said active operation mode, a second pair of a
8 high potential and a low potential having a potential
9 difference larger than that of said first potential pair,
10 wherein a substrate potential of an MIS transistor in
11 said first logic gate and that of an MIS transistor in said
12 second logic gate are common to each other, and
13 at least said first logic gate includes an MIS
14 transistor to which a substrate bias is applied in a
15 reverse direction by said substrate potential.

C3

1 16. (Amended) A semiconductor integrated circuit
2 comprising:
3 a first logic gate connected to a first pair of a high
4 potential line and a low potential line in an active
5 operation mode; and
6 a second logic gate connected to a second pair of a
7 high potential line and a low potential line in said active
8 operation mode, said second line pair having a potential
9 difference larger than that of said first potential line
10 pair,

C3
comp

11 wherein a substrate potential line is commonly used
12 for supplying a substrate potential to an MIS transistor of
13 said first logic gate and for supplying a substrate
14 potential to an MIS transistor of said second logic gate,
15 and
16 at least said first logic gate includes an MIS
17 transistor to which a substrate bias is applied in a
18 reverse direction by said substrate potential.

C4

1 20. (Amended) A semiconductor integrated circuit
2 having a circuit region in which a number of logic gates
3 each having an MIS transistor are arranged on a
4 semiconductor substrate,
5 wherein said circuit region has a well region
6 including portions shared by a substrate potential for each
7 conduction type of MIS transistor,
8 a first logic gate using, as an operation power source
9 in an active operation mode, a first pair of potentials
10 having a relatively small potential difference and a second
11 logic gate using, as an operation power source in said
12 active operation mode, a second pair of potentials having a
13 relatively large potential difference are formed in said
14 well region,

C4
Coul

15 in said well region, a p-type well portion in which an
16 n-channel type MIS transistor is formed and an n-type well
17 portion in which a p-channel type MIS transistor is formed
18 are adjacent to each other, and
19 metal lines for supplying said first pair of
20 potentials, said second pair of potentials, and substrate
21 potentials are arranged on said well region.

sub
D10

1 37. (Amended) A design data recording medium on which
2 design data for forming an integrated circuit on a
3 semiconductor chip is recorded so as to be readable by a
4 computer, the design data comprising:
5 first mask pattern data for determining a figure
6 pattern for forming a first logic gate to which an
7 operation power source is supplied, in an active operation
8 mode, from a first pair of potential lines having a
9 relatively small potential difference and a substrate
10 potential is supplied from a substrate potential line on
11 said semiconductor chip; and
12 second mask pattern data for determining a figure
13 pattern for forming a second logic gate to which an
14 operation power source is supplied, in said active
15 operation mode, from a second pair of potential lines

C6

*sub
Dro
cont'd*

16 having a relatively large potential difference and a
17 substrate potential is supplied from a substrate potential
18 line.

1 38. (Amended) A design data recording medium on which
2 design data for designing an integrated circuit to be
3 formed on a semiconductor chip is recorded so as to be
4 readable by a computer, the design data comprising:

*CB
cont'd*

5 first function description data for determining a
6 function of a first logic gate to which an operation power
7 source is supplied, in an active operation mode, from a
8 first pair of potential lines having a relatively small
9 potential difference and a substrate potential is supplied
10 from a substrate potential line; and

11 second function description data for determining a
12 function of a second logic gate to which an operation power
13 source is supplied, in said active operation mode, from a
14 second pair of potential lines having a relatively large
15 potential difference and a substrate potential is supplied
16 from a substrate potential line connected to said substrate
17 potential line.
